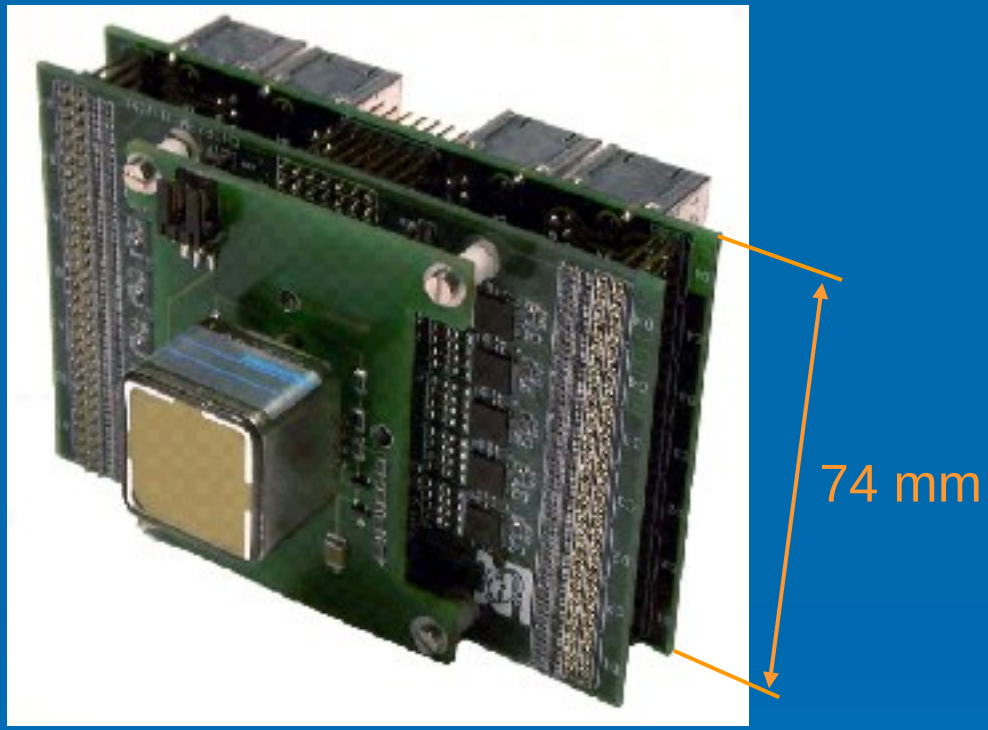
TS/CV/DC CFD Team

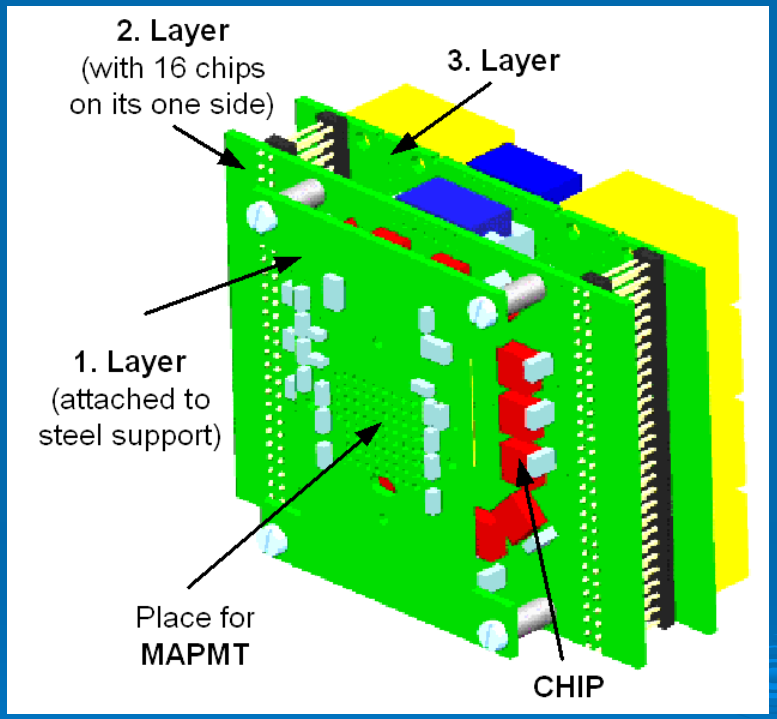


Thermal behavior of the LHCb PS VFE Board

Vaclav Vins

THE PROBLEM

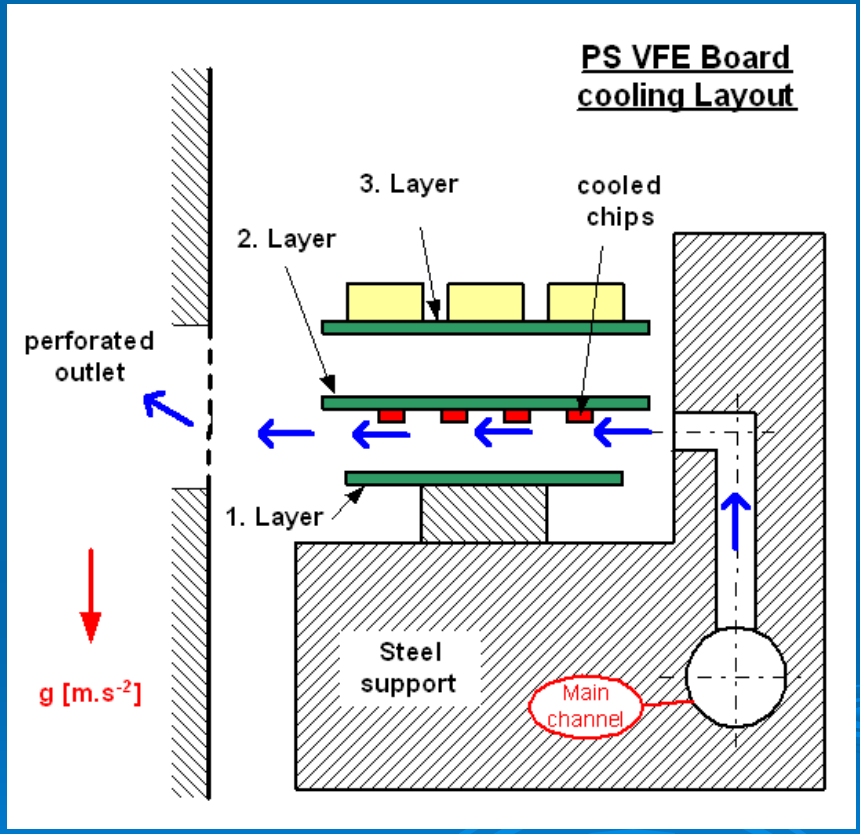
- The main goal of this project is study of the air-flow used for cooling of electronics device installed at PS part of LHCb Detector
- PS VFE Board consists of three main layers. 16 chips which should be cooled down with the dry air-flow are installed on bottom side of the second (middle) layer
- The Board itself is attached on the specially designed steel support with air distribution channels inside



PS VFE Board

MAIN PARAMETERS

- Primary parameters to be solved:
  - Necessary **minimum mass flow rate** of the cooling air
  - Optimize position and main dimensions of the air-flow inlets
- Main technical data:
  - Heat power in one PS Board … 8 W (0,5 W per each chip)
  - Maximum reasonable temperature of the chip surface … + 50 C
  - Inlet air-flow temperature … ambient temperature (around + 22 C)



Scheme of the cooling layout

Vaclav Vins

THE CFD MODEL

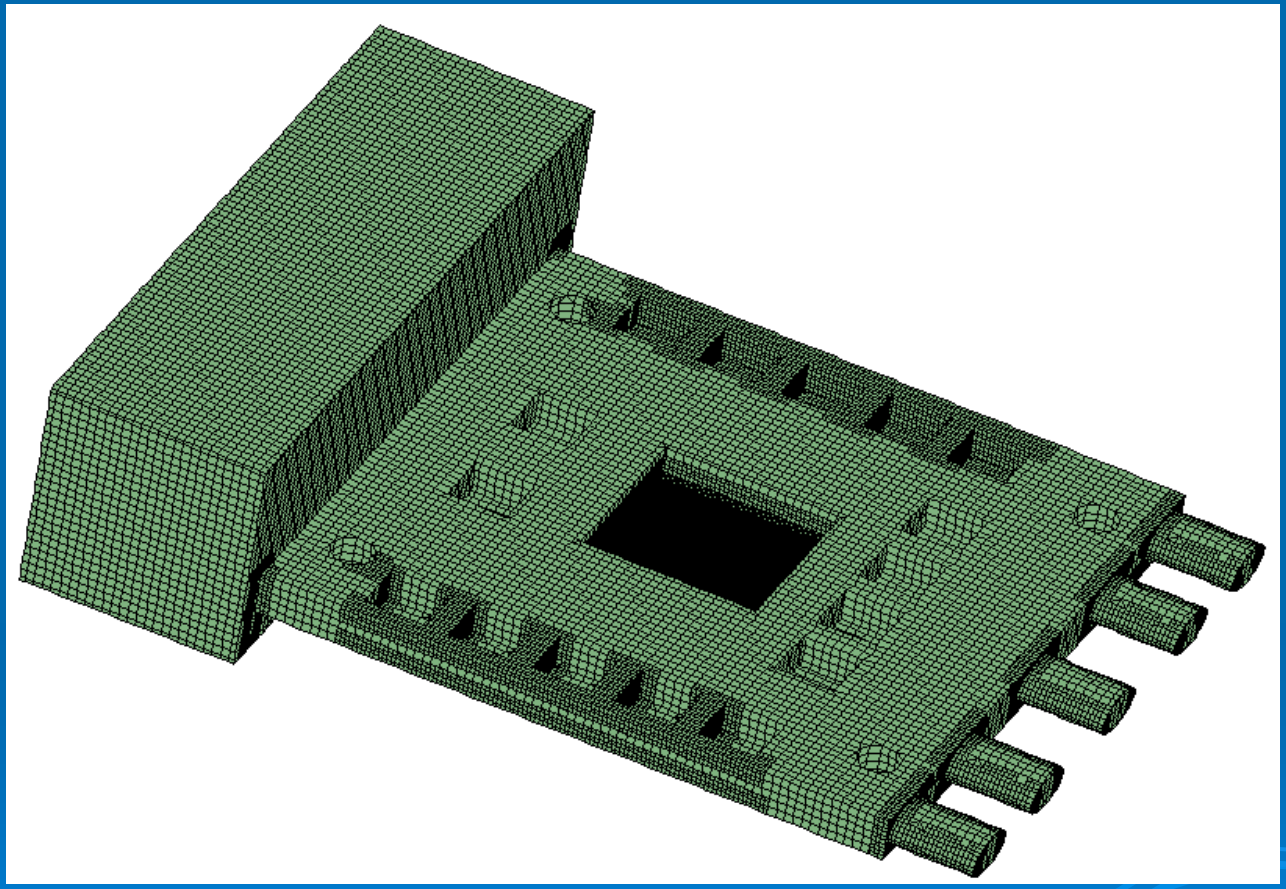
MESH:

- Geometry of the problem was defined and simplified on the base of CATIA technical drawing
- Only the volume area between first and second layer of PS VFE Board and the outlet region are modeled
- Assumed number of the cells … around 200 000

SOLUTION ASSUMPTIONS:

- Steady state case (time independent) is being solved
- Turbulent flow with high Reynolds number is put into account
- Except chips all other walls are assumed as adiabatic

GENERATED MESH

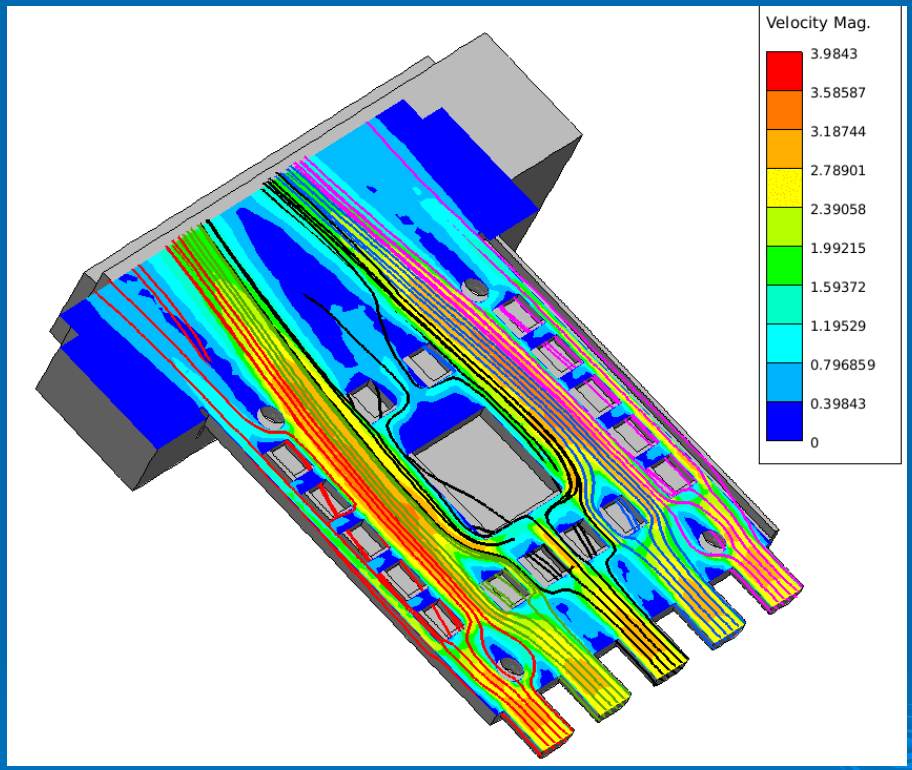


Generated mesh of the problem with hexahedral cells

Vaclav Vins

EXPECTED RESULTS

- The problem is still being solved
- Studied variables:
  - Chip surface temperature
  - Properties of the Air-flow (velocity field, pressure …)
- Final results:
  - The necessary mass flow rate
  - Inlets configuration



Some results obtained from first approximate solution (Velocity magnitude field)

Vaclav Vins